AMENDMENTS TO THE SPECIFICATION:

Kindly replace the paragraph beginning at page 27, line 5, with the following amended paragraph:

The external device controller 302 is input with an address signal [[313]] 314 indicating an SDRAM bank address in the E bus address signal bus 151 (hereinafter, "SDRAM bank address signal"). The external device controller 302 issues a pre-read data memory control signal 312 for controlling the pre-read data storages 303 and 304.

Kindly replace the paragraph bridging pages 27 and 28, with the following amended paragraph:

After having performed the read access, if the next access request is not issued, the external device controller 302 issues an instruction to the external address generator 112 based on the SDRAM bank address signal [[313]] 314 in the same manner as in the first embodiment, so that the next address is generated by incrementing or decrementing the address used in the first access. The external device controller 302 controls the read access of the external device 113 by this address. The read data is held in the pre-read data storage 303.